IN THE CLAIMS

Please amend the claims as follows:

Claims 1-20 (Canceled).

Claim 21 (New) A semiconductor integrated circuit comprising:

circuits having a certain function;

a plurality of input terminals which receive input data to said circuits from outside;

a plurality of output terminals which output data output from said circuits to the outside;

a plurality of first registers connected in series, said plurality of first registers shifting stored data to respective adjacent registers in sequence, and said plurality of first registers being connected in one-to-one correspondence to said plurality of input terminals or to said plurality of output terminals;

a plurality of second registers connected in series, said plurality of second registers shifting stored data to respective adjacent registers in sequence, and said plurality of second registers being connected in one-to-one correspondence to said plurality of input terminals or to said plurality of output terminals;

a first scan input terminal formed at one end of said plurality of first series-connected registers;

a first scan output terminal formed at another end of said plurality of first series-connected registers, said first scan output terminal being placed at an end portion;

a second scan input terminal formed at one end of said plurality of second series-connected registers, said second scan input terminal being placed at the end portion at which the first scan output terminal is placed; and

a second scan output terminal formed at the other end of said plurality of second series-connected registers.

Claim 22 (New) The semiconductor integrated circuit according to claim 21, further comprising a line formed between said first scan output terminal and said second scan input terminal.

Claim 23 (New) The semiconductor integrated circuit according to claim 21, wherein said circuits, said plurality of input terminals, said plurality of output terminals, said plurality of first and second registers, said first scan input terminal, said first scan output terminal, said second scan input terminal, and said second scan output terminal configure a first integrated circuit, and a second integrated circuit having an arrangement which is a mirror inversion of said first integrated circuit is placed on a side of said first integrated circuit.

Claim 24 (New) The semiconductor integrated circuit according to claim 21, wherein said circuits comprise:

a memory cell array in which a plurality of memory cells are arrayed in row and column directions;

a row decoder which selects said memory cells arrayed in the row direction;

a column decoder which selects said memory cells arrayed in the column direction; and

a sense amplifier which reads out data from a selected memory cell.

Claim 25 (New) The semiconductor integrated circuit according to claim 21, wherein an identical data line is connected to adjacent first and second registers of said plurality of

first and second registers, data is input to one of the adjacent first and second registers from the outside of the circuits, and the data is output from the other of the adjacent first and second registers to the outside of the circuits.

Claim 26 (New) A semiconductor integrated circuit comprising:

circuits having a certain function which are formed in a four-sided figure including first, second, third and fourth sides;

a plurality of input terminals formed near the first side of the four-sided figure, which receive input data to said circuits from the outside;

a plurality of output terminals formed near the first side of the four-sided figure, which output data output from said circuits to the outside;

a plurality of first registers connected in series formed in the four-sided figure, said plurality of first registers shifting stored data to respective adjacent registers in sequence, and said plurality of first registers being connected in one-to-one correspondence to said plurality of input terminals or to said plurality of output terminals;

a plurality of second registers connected in series formed in the four-sided figure, said plurality of second registers shifting stored data to respective adjacent registers in sequence, and said plurality of second registers being connected in one-to-one correspondence to said plurality of input terminals or to said plurality of output terminals;

a first scan input terminal formed at one end of said plurality of first series-connected registers, said first scan input terminal being placed near the second side forming an angle with the first side;

a first scan output terminal formed at another end of said plurality of first series-connected registers, said first scan output terminal being placed near the third side opposite to the second side;

a second scan input terminal formed at one end of said plurality of second series-connected registers, said second scan input terminal being placed near the third side; and

a second scan output terminal formed at another end of said plurality of second series-connected registers, said second scan output terminal being placed near the second side.

Claim 27 (New) The semiconductor integrated circuit according to claim 26, further comprising an operation control circuit which controls operations of said circuits and said plurality of first and second registers.

Claim 28 (New) The semiconductor integrated circuit according to claim 27, wherein said operation control circuit comprises:

a plurality of third and fourth registers connected to input and output terminals;

a third scan input terminal connected to one end of said plurality of third registers;

a third scan output terminal connected to another end of said plurality of third registers;

a fourth scan input terminal connected to one end of said plurality of fourth registers; and

a fourth scan output terminal connected to another end of said plurality of fourth registers,

wherein said third scan input terminal is connected to said first scan output terminal, and said fourth scan output terminal is connected to said second scan input terminal.

Claim 29 (New) The semiconductor integrated circuit according to claim 28, wherein said third scan output terminal and said fourth scan input terminal are arranged adjacent to each other in a same end portion, and said semiconductor integrated circuit further comprises a line formed between said third scan output terminal and said fourth scan input terminal.

Claim 30 (New) The semiconductor integrated circuit according to claim 27, wherein said circuits, said plurality of input terminals, said plurality of output terminals, said plurality of first and second registers, said first scan input terminal, said first scan output terminal, said second scan input terminal, and said second scan output terminal configure a first integrated circuit, said operation control circuit is placed adjacent to said first integrated circuit, and a second integrated circuit having an arrangement which is a mirror inversion of said first integrated circuit is placed on a side of said operation control circuit away from a side at which said first integrated circuit is formed.

Claim 31 (New) The semiconductor integrated circuit according to claim 26, wherein said circuits comprise:

a memory cell array in which a plurality of memory cells are arrayed in row and column directions;

a row decoder which selects said memory cells arrayed in the row direction;

a column decoder which selects said memory cells arrayed in the column direction; and

a sense amplifier which reads out data from a selected memory cell.

Claim 32 (New) The semiconductor integrated circuit according to claim 26, wherein an identical data line is connected to adjacent first and second registers of said plurality of

first and second registers, data is input to one of the adjacent first and second registers from the outside of the circuits, and the data is output from the other of the adjacent first and second registers to the outside of the circuits.

Claim 33 (New) A semiconductor integrated circuit comprising:

a first integrated circuit including:

circuits having a certain function;

a plurality of input terminals which receive input data to said circuits from outside;

a plurality of output terminals which output data output from said circuits to the outside;

a plurality of first registers connected in series, said plurality of first registers shifting stored data to respective adjacent registers in sequence, and said plurality of first registers being connected in one-to-one correspondence to said plurality of input terminals or to said plurality of output terminals;

a plurality of second registers connected in series, said plurality of second registers shifting stored data to respective adjacent registers in sequence, and said plurality of second registers being connected in one-to-one correspondence to said plurality of input terminals or to said plurality of output terminals;

a first scan input terminal formed at one end of said plurality of first series-connected registers;

a first scan output terminal formed at the other end of said plurality of first series-connected registers, said first scan output terminal being placed at an end portion;

a second scan input terminal formed at one end of said plurality of second series-connected registers, said second scan input terminal being placed at the end portion at which the first scan output terminal is placed; and

a second scan output terminal formed at another end of said plurality of second series-connected registers,

a first operation control circuit placed adjacent to one end of said first integrated circuit, said first operation control circuit controlling operations of said circuits and said plurality of first and second registers;

a second integrated circuit having an arrangement which is a mirror inversion of said first integrated circuit with respect to a straight line passing through a region which is outside of the first operation control circuit and which is located away from a side at which the first integrated circuit is formed; and

a second operation control circuit having an arrangement which is a mirror inversion of the first operation control circuit with respect to the straight line.

Claim 34 (New) The semiconductor integrated circuit according to claim 33, wherein said first operation control circuit comprises:

a plurality of third and fourth registers connected to the input and output terminals;

a third scan input terminal connected to one end of said plurality of third registers;

a third scan output terminal connected to another end of said plurality of third registers;

a fourth scan input terminal connected to one end of said plurality of fourth registers; and

a fourth scan output terminal connected to another end of said plurality of fourth registers,

wherein said third scan input terminal is connected to said first scan output terminal, and said fourth scan output terminal is connected to said second scan input terminal.

Claim 35 (New) The semiconductor integrated circuit according to claim 34, wherein said third scan output terminal and said fourth scan input terminal are arranged adjacent to each other in a same end portion.

Claim 36 (New) The semiconductor integrated circuit according to claim 35, wherein said second operation control circuit includes a fifth scan input terminal and a fifth scan output terminal, and said semiconductor integrated circuit further comprises a first line connecting said third scan output terminal and said fifth scan input terminal and a second line connecting said fifth scan output terminal and said fourth scan input terminal.

Claim 37 (New) The semiconductor integrated circuit according to claim 36, wherein said first line and said second line cross.

Claim 38 (New) The semiconductor integrated circuit according to claim 33, wherein said circuits comprise:

a memory cell array in which a plurality of memory cells are arrayed in row and column directions;

a row decoder which selects said memory cells arrayed in the row direction;

a column decoder which selects said memory cells arrayed in the column direction; and

a sense amplifier which reads out data from a selected memory cell.

Claim 39 (New) The semiconductor integrated circuit according to claim 33, wherein an identical data line is connected to adjacent first and second registers of said plurality of first and second registers, data is input to one of the adjacent first and second registers from the outside of the circuits, and the data is output from the other of the adjacent first and second registers to the outside of the circuits.

Claim 40 (New) A semiconductor integrated circuit comprising:

circuits having a certain function;

a plurality of input terminals which receive input data to said circuits from outside;

a plurality of output terminals which output data output from said circuits to the outside;

a plurality of first registers connected in series, said plurality of first registers shifting stored data to respective adjacent registers in sequence, and said plurality of first registers being connected in one-to-one correspondence to said plurality of input terminals or said plurality of output terminals;

a plurality of second registers connected in series, said plurality of second registers shifting stored data to respective adjacent registers in sequence, and said plurality of second registers being connected in one-to-one correspondence to said plurality of input terminals or said plurality of output terminals;

a first scan input terminal formed at one end of said plurality of first series-connected registers, said first scan input terminal being placed at an end portion;

a first scan output terminal formed at one end of said plurality of second series-connected registers, said first scan output terminal being placed at the end portion at which the first scan input terminal is placed;

a line formed between another end of said plurality of first series-connected registers and another end of said plurality of second series-connected registers; and

an operation control circuit formed in a four-sided figure including first, second, third and fourth sides, which controls operations of said circuits and said plurality of first and second registers, said first side of the four-sided figure in which the operation control circuit is formed being placed adjacent to the end portion at which the first scan input terminal and first scan output terminal are placed, said operation control circuit including a second scan input terminal connected to the first scan input terminal and a second scan output terminal connected to the first scan output terminal, and said second scan output terminal being placed near the second side opposite to the first side.

Claim 41 (New) The semiconductor integrated circuit according to claim 40, wherein the operation control circuit includes a third scan input terminal placed near the second side different from the first side, a third scan output terminal placed near the third side and a line connecting the third scan input terminal and the third scan output terminal.

Claim 42 (New) The semiconductor integrated circuit according to claim 40, wherein said circuits, said plurality of input terminals, said plurality of output terminals, said plurality of first and second registers, said first scan input terminal, said first scan output terminal, and said line configure a first integrated circuit, and a second integrated circuit having an arrangement which is a mirror inversion of said first integrated circuit is placed on a side of said operation control circuit away from a side at which said first integrated circuit is formed.

Claim 43 (New) The semiconductor integrated circuit according to claim 40, wherein said circuits comprise:

a memory cell array in which a plurality of memory cells are arrayed in row and column directions;

a row decoder which selects said memory cells arrayed in the row direction;

a column decoder which selects said memory cells arrayed in the column direction; and

a sense amplifier which reads out data from a selected memory cell.

Claim 44 (New) The semiconductor integrated circuit according to claim 40, wherein an identical data line is connected to adjacent first and second registers of said plurality of first and second registers, data is input to one of the adjacent first and second registers from the outside of the circuits, and the data is output from the other of the adjacent first and second registers to the outside of the circuits.

Claim 45 (New) A semiconductor integrated circuit comprising:

a first integrated circuit including:

circuits having a certain function;

a plurality of input terminals which receive input data to said circuits from outside;

a plurality of output terminals which output data output from said circuits to the outside;

a plurality of first registers connected in series, said plurality of first registers shifting stored data to respective adjacent registers in sequence, and said plurality of first registers being connected in one-to-one correspondence to said plurality of input terminals or to said plurality of output terminals;

a plurality of second registers connected in series, said plurality of second registers shifting stored data to respective adjacent registers in sequence, and said plurality of second registers being connected in one-to-one correspondence to said plurality of input terminals or to said plurality of output terminals;

a first scan input terminal formed at one end of said plurality of first series-connected registers, said first scan input terminal being placed at an end portion;

a first scan output terminal formed at one end of said plurality of second series-connected registers, said first scan output terminal being placed at the end portion at which the first scan input terminal is placed; and

a line formed between another end of the plurality of first series-connected registers and another end of the plurality of second series-connected registers,

an operation control circuit placed adjacent to one end of said first integrated circuit, said operation control circuit controlling operations of said circuits and said plurality of first and second registers; and

a second integrated circuit having an arrangement which is a mirror inversion of said first integrated circuit, said second integrated circuit being placed on a side of said operation control circuit away from a side at which said first integrated circuit is formed.

Claim 46 (New) The semiconductor integrated circuit according to claim 45, wherein said operation control circuit includes:

a second scan input terminal to which data is input;

a second scan output terminal connected to the second scan input terminal;

a plurality of second input terminals which input data;

a plurality of second output terminals which output data;

a plurality of third registers connected in series, said plurality of third registers shifting stored data to respective adjacent registers in sequence, and said plurality of third registers being connected in one-to-one correspondence to said plurality of second input terminals or to said plurality of second output terminals;

a third scan input terminal connected to one end of said plurality of third registers; and

a third scan output terminal connected to another end of said plurality of third registers,

wherein said second scan output terminal is connected to said first scan input terminal, and said third scan input terminal is connected to said first scan output terminal.

Claim 47 (New) The semiconductor integrated circuit according to claim 45, wherein said operation control circuit comprises:

a memory cell array in which a plurality of memory cells are arrayed in row and column directions;

a row decoder which selects said memory cells arrayed in the row direction;

a column decoder which selects said memory cells arrayed in the column direction; and

a sense amplifier which reads out data from a selected memory cell.

Claim 48 (New) The semiconductor integrated circuit according to claim 45, wherein an identical data line is connected to adjacent first and second registers of said plurality of first and second registers, data is input to one of the adjacent first and second registers from the outside of the circuits, and the data is output from the other of the adjacent first and second registers to the outside of the circuits.

Claim 49 (New) A semiconductor integrated circuit comprising:

circuits having a certain function;

a plurality of input terminals which receive input data to said circuits from outside;

a plurality of output terminals which output data output from said circuits to the outside;

a plurality of first registers connected in series, said plurality of first registers shifting stored data to respective adjacent registers in sequence, and said plurality of first registers being connected in one-to-one correspondence to said plurality of input terminals or to said plurality of output terminals;

a plurality of second registers connected in series, said plurality of second registers shifting stored data to respective adjacent registers in sequence, and said plurality of second registers being connected in one-to-one correspondence to said plurality of input terminals or to said plurality of output terminals;

a first scan input terminal formed at one end of said plurality of first series-connected registers, said first scan input terminal being placed at an end portion;

a first scan output terminal formed at one end of said plurality of second series-connected registers, said first scan output terminal being placed at the end portion at which the first scan input terminal is placed; and

a line formed between another end of the plurality of first series-connected registers and another end of the plurality of second series-connected registers,

wherein an identical data line is connected to adjacent first and second registers of said plurality of first and second registers, data is input to one of the adjacent first and second registers from the outside of the circuits, and the data is output from the other of the adjacent first and second registers to the outside of the circuits.

Claim 50 (New) The semiconductor integrated circuit according to claim 49, further comprising an operation control circuit which controls operations of said circuits and said plurality of first and second registers.

Claim 51 (New) The semiconductor integrated circuit according to claim 50, wherein said operation control circuit comprises:

a second scan input terminal to which data is input;

a second scan output terminal connected to the second scan input terminal;

a plurality of third registers connected to both an input terminal and an output terminal;

a third scan input terminal connected to one end of said plurality of third registers; and

a third scan output terminal connected to another end of said plurality of third registers,

wherein said second scan output terminal is connected to said first scan input terminal, and said third scan input terminal is connected to said first scan output terminal.

Claim 52 (New) The semiconductor integrated circuit according to claim 50, wherein said circuits, said plurality of input terminals, said plurality of output terminals, said plurality of first and second registers, said first scan input terminal, said first scan output terminal, and said line configure a first integrated circuit, and a second integrated circuit having an arrangement which is a mirror inversion of said first integrated circuit is placed on a side of said operation control circuit away from a side at which said first integrated circuit is formed.

Claim 53 (New) The semiconductor integrated circuit according to claim 49, wherein said circuits comprise:

a memory cell array in which a plurality of memory cells are arrayed in row and column directions;

a row decoder which selects said memory cells arrayed in the row direction;

a column decoder which selects said memory cells arrayed in the column direction; and

a sense amplifier which reads out data from a selected memory cell.